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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,164	08/25/2000	Yih-Feng Chyan	15-6-9	6246
7590	05/05/2004		EXAMINER	
AGERE SYSTEMS INC. 4 Connell Drive Room 4U-533C Berkeley Heights, NJ 07922-2747				DICKEY, THOMAS L
		ART UNIT	PAPER NUMBER	2826

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/648,164	CHYAN ET AL.
	Examiner Thomas L Dickey	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 March 2004.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 15-19 is/are allowed.

6) Claim(s) 1-4, 10, 13 and 14 is/are rejected.

7) Claim(s) 5-9, 11 and 12 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 16 July 2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) Interview Summary (PTO-413) Paper No(s). _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

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DETAILED ACTION

1. The amendment filed on 03/05/2004 has been entered.

Drawings

2. The formal drawings filed on 07/10/2002 are acceptable.

Information Disclosure Statement

3. If applicants are aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

4. The disclosure is objected to because of the following informalities:

- A. On page 3 line 20 Applicants refer to "U.S. Serial number 290533." This reference misidentifies application number 09/335,646 filed 6/18/99, and must be corrected. The correction should take the form of instructions such as:

On page 3 line 20 of the originally filed specification, replace "U.S. Serial number 290533" with – U.S. Serial number 09/335,646 filed 6/18/99, now abandoned–

- B. On page 3 line 26 Applicants refer to "U.S. Serial number 341,190." This reference misidentifies application number 09/528,753 filed 03/20/2000, and must be corrected. The correction should take the form of instructions such as:

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On page 3 line 26 of the originally filed specification, replace "U.S. Serial number 341,190" with – U.S. Serial number 09/528,753 filed 03/20/2000, now U.S. Patent Number 6,518,622 –

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4,10,13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over ONO et al. (6,642,575) in view of MAZURE et al. (5,398,200).

Ono et al. discloses an integrated circuit structure comprising a semiconductor layer 50 having a major surface formed along a plane; first 54 and second 65 spaced-apart doped regions extending into the surface from the plane; a monocrystalline third region 58 positioned above the plane and over the first region 54; and a conductive layer 73 between the first and second region 65s and above the plane, providing electrical connection between the doped regions, wherein the first doped region 54 is the first source/drain region, and the third region 58 is the channel region, of a first MOSFET (formed by source 54 channel 58 drain 57 and gate 63), the second region 65 is part of a transistor, specifically the source/drain region of a second MOSFET (formed by source 65 channel 53 drain not numbered, n type region opposite source 65, and gate 62), said structure further comprising a channel region

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53 of the second MOSFET aligned with the second source/drain region, and wherein the diffusion regions are configured (combined with parts 61-52-64) to form an inverter circuit and the conductive layer 73 is a continuous film extending from the first region 54 to the second region 65 and physically contacting the first region 54 and the second region 65. Note figures 7 and 8f-8l, column 13 lines 33-55, and column 14 lines 1-48 of Ono et al. Ono et al. does not disclose that the monocrystalline third region is a doped region of different conductivity type than the first region. However, Mazure et al. discloses an integrated circuit structure with a first spaced-apart doped region 14 extending into a surface from a plane and a monocrystalline third region 30 positioned above the plane and over the first region 14, wherein the monocrystalline third region 30 is a doped region of different conductivity type than the first region 14. Note figure 4 and column 4 lines 30-68, especially lines 63-66, of Mazure et al. The reason for doping third region 30 to a different conductivity type from first region 14, as Mazure et al. explains at column 5 line 1, is to use region 30 as the channel of a MOSFET. Doping the channel, as Mazure et al. points out at column 5 lines 1-3, has the advantageous result that the threshold (turn-on) voltage of that MOSFET may be adjusted up or down by increasing or decreasing the doping level of the monocrystalline third region 30. Therefore, it would have been obvious to a person having skill in the art to replace the monocrystalline third region of Ono et al.'s integrated circuit structure with the doped monocrystalline third region of

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different conductivity type than the first region such as taught by Mazure et al. in order to dope the third region into a channel region of different conductivity type from the first region to thus provide the ability to adjust the threshold voltage of the MOS-FET thus formed by the first and third regions.

Allowable Subject Matter

6. Claims 15-18 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising a first layer of semiconductor material; a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and a conductive layer in a plane extending between the first layer and the first field effect transistor channel region, said conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, as recited in claim 15.

Claim 19 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semi-

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conductor device comprising: a first layer of semiconductor material; a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and a conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, wherein the conductive layer comprises a metal silicide.

Claims 5-9,11, and 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-4,10,13, and 14 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Mon-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
04/2004

Minhloan Tran
Minhloan Tran
Primary Examiner
Art Unit 2826